



## **ADVANCED 15-LEVEL INVERTER DESIGN FOR SOLAR PV INTEGRATION**

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### **ABSTRACT**

A new 15 level inverter is presented in the paper to improve the solar photovoltaic (PV) grid integration process. Improved substantially in the pattern of waves quality with the current THD 3.91%, and voltage THD to 15.77%. Due to its efficiency the design is able to achieve a power conversion efficiency level of 96.75%. The reductions in switches to seven devices is successful and allows for the operational simplicity and cost effectiveness. MATLAB/Simulink simulations have been used to comprehensively revalued the suggested inverter design performance in terms of its operational characteristics and functionality. And the simulation tests looked into analyzing the PV grid connect while considering a group of operational conditions. The results of the test indicate that the proposed system will be able to operate in real life condition because it provides good results in terms of grid stability and dependability with a smooth connection to the grid. Improvements in inverter technology to achieve high efficiency would be facilitated by research presented here that further refines integration



method for solar PV systems that requires less operational complexity and better grid integration.

**KEYWORDS**

Alternate Phase Opposition Disposition (APOD); Efficiency; Inverter; Photovoltaic; Pulse Width Modulation (PWM); Total Harmonic Distortion (THD).

## 1. INTRODUCTION

Multilevel inverters produce multiple alternating current (AC) voltage levels by uniting a number of direct current (DC) sources along with capacitors. These inverters operate with staircase-like waveforms to minimize electromagnetic interference and decrease voltage strain and increase DC to AC power conversion effectiveness across multiple applications. Multilevel inverters supply power through multiple voltage stages yet conventional two-level inverters work with a single voltage source (He and Ye, 2023). The output waveform synthesis to different voltage levels becomes possible through power device state modifications that produce stepped approximations to sinusoidal waveforms. The neutral point clamped (NPC) inverter functions as one of the primary multilevel inverter topologies which produces intermediate voltages through capacitors that connect the DC source to the ground. The cascaded h-bridge (CHB) inverter demonstrates popularity since it utilizes multiple H-bridge cells to develop stepped voltage outputs. The reduced voltage challenge on power devices enhances switching efficiency along with an improvement in power conversion systems' overall efficiency (Khoun-Jahan, 2021; Akbari and Ebrahimi, 2022).

Multilevel inverters are becoming more common because semiconductor technology improvements and control strategy developments occurred. Modern control methods through pulse width modulation (PWM) schemes combined with modulation algorithms let operators precisely control the output waveform thus maximizing both performance and reliability of inverters. Power conversion systems are currently benefitting greatly from modified PWM approaches due to their significant role in enhancing efficiency and reducing harmonics and improving system performance in multilevel inverters. The purpose of this literature review is to investigate modified PWM techniques in multilevel inverters by analyzing their benefits along with their drawbacks and present applications (Khoun-Jahan, 2021; Suresh and Parimalasundar, 2022). The THD decreases and harmonic dispersion enhances through modified forms of carrier base pulse width modulation (CBPWM) techniques including phase-shifted PWM (PSPWM) and level-shifted PWM (LSPWM) that modify either carrier signal phase or signal levels. Multilevel inverters mainly depend on SVPWM to create voltage switching sequences through their space vector representations. The modified PWM techniques MSVPWM and SHEPWM enable better output waveform quality by making selective voltage level adjustments (Liu et al, 2022).

The carrier wave frequency controls the inverter switching frequency operation in SPWM systems yet the sinusoidal reference wave defines the output voltage waveform. The state-change of the switch produces output pulses at the inverter when the reference signal exceeds

the carrier wave's current value. SPWM allows users to modify modulation index and carrier frequency parameters for the purpose of adjusting output voltage levels and enhancing harmonic performance. Phase-shifted PWM schemes and level-shifted PWM schemes represent additional methods of operation. By shifting the carrier signals for each phase leg Phase-shifted PWM decreases the amount of harmonics in the output (Abdul-Abbas and Salih, 2021; Anssari, 2021). Using level-shifted PWM techniques allows carriers to split by voltage levels in order to create cascading waveforms which reduce harmonics while maintaining constant switching frequency. Performance optimization of multilevel inverter (MLI) systems (Al-Hitmi, 2023; Jena and Kumar, 2023) depends on the chosen method yet these approaches will differ according to application requirements which include operating efficiency together with thermal management along with THD.

Issues with the implementation of the complex 15 level inverter as a method of interfacing the solar PV systems are addressed. However, the control system for the different voltage levels has to follow grid requirements, which is the main hurdle of achieving it. At the end cascaded layers are dependent upon exact control algorithms that are used to make sure voltage balance between the layers. The technical demands are reducing the switching losses as well as keeping the system efficiency very high. Adaptive maximum power point tracking (MPPT) algorithms are needed for connectivity of PV systems under varying irradiance condition. Advanced control methods together with very strong hardware design and optimized system level implementation (Sarebanzadeh, 2021; Suresh and Sujatha, 2023) is required for successful implementation of solar PV into the grid with a 15-level inverter topology.

Artificial intelligence (AI) and machine learning (ML) systems have revolutionized various industrial processes to optimize real-time control systems and forecast maintenance needs as well as identify potential equipment failures. Tools achieve better outcomes when they operate with large databases which contain high-quality information (Tak and Chattopadhyay, 2022; Liu et al, 2022; Jena and Kumar, 2023). Acquiring datasets for power electronics systems such as MLIs becomes difficult through tests on hardware because they are expensive with operators facing physical constraints. The unknown circumstances involving component deterioration combined with grid failures make ML models susceptible to incorrect predictions and operation instability. Complex control procedure designs create substantial issues for developers during their development phase. Developers need to find proper ratios between computation speed and accuracy results when using intelligent control methods that incorporate fuzzy logic controllers neural networks and reinforcement learning (Abdul-Abbas and Salih, 2021). Although digital signal processors and field-programmable gate arrays execute these algorithms there exists a

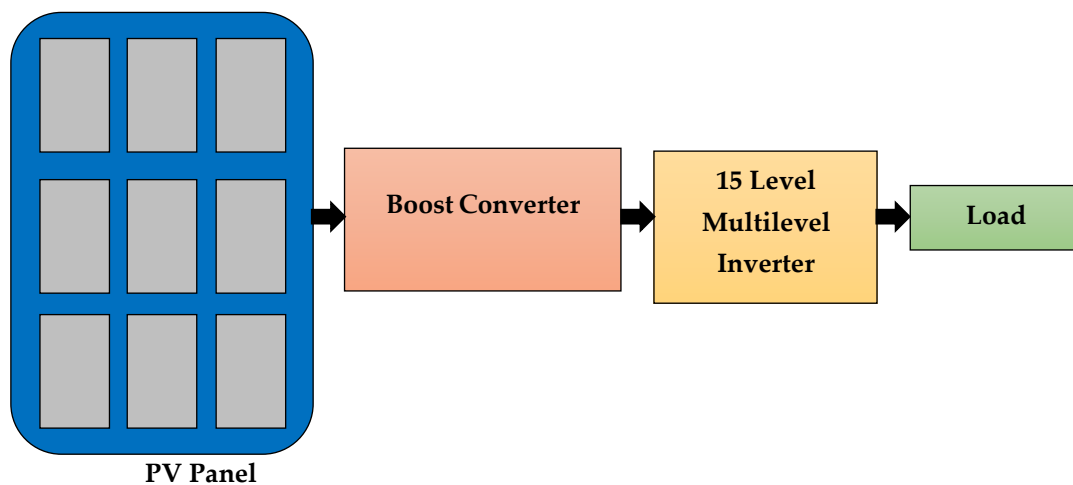
constraint on their computation capacity. Stable control solutions need development to ensure adaptability during changing conditions while maintaining inverter dynamic performance and minimally affecting THD and additional strategies which researchers currently investigate. In terms of grid integration MLIs must follow grid codes by demonstrating three capabilities known as fault ride-through and power factor adjustment and voltage and frequency stability. Intelligent systems face significant challenges when performing these tasks especially when applied to microgrid and weak grid systems. The utilization of AI models in controlling power systems encounters operational complications since it becomes challenging to ensure grid synchronization while making clean transitions between being grid-connected and operating independently (Akbari and Ebrahimi, 2022; Al-Jabari et al, 2024; Akbari and Ebrahimi, 2022). A comprehensive list of vital elements exists for this proposed inverter system used in renewable energy applications:

- An improved 15-level inverter design aims to develop both current and voltage THD levels extremely low to enhance grid compatibility and solar PV integration along with improving waveform quality.
- The design implementation of seven switches enables exceptional efficiency marking as an indicator of improved power conversion performance at reduced costs and simple operations.
- MATLAB/Simulink simulations analyze the suggested inverter design from multiple operation viewpoints with special attention to PV system integration to the grid and overall performance behavior.
- The proposed inverter solution necessitates stability, dependability and grid-to-grid interaction assessments to determine outcomes with promising data that help in actual implementations and operational reliability.
- The invention provides an excellent solution for solar PV integration to enhance efficiency by simplifying structure while boosting functionality and unifying grid relationship which promotes sustainable and dependable renewable energy deployment.

## **2. FIFTEEN LEVEL INVERTER WITH PV INTEGRATION**

The 15-level Multilevel Inverter requires seven switches, three diodes and three voltage sources to work in its different operation modes. Six switches work actively with one diode in each phase to create eight voltage levels in basic operation. The three engaged voltage sources push the system into boost mode to generate three further voltage outputs. To achieve the additional three voltage levels the inverter model uses one broken voltage source combined with switch

modifications. The inverter can use the full bridge rectifier to switch on the diodes and produce three output voltage levels. A PV panel is integrated with a regulated converter to supply regulated DC voltage at symmetrical 32 V to a 15-level inverter. The primary objective is to minimize the number of power switches, optimizing system efficiency and performance. The boost converter facilitates stepping up the PV panel's output voltage to match the required input for the 15-level MLI. This combined system ensures efficient power conversion, enabling the generation of high-quality AC waveforms with reduced THD. Integrating these components allows for seamless grid connection, optimizing energy transfer while leveraging the advantages of multilevel inverter technology for enhanced grid compatibility and improved renewable energy utilization. The novelty of the 15-level inverter design achieves a significant reduction in power switches, requiring only 7 compared to the 24 switches in existing cascaded topologies. This reduction enables a streamlined system with only 7 driver circuits and facilitates achieving low THD levels. This paper introduces a level-15 multilevel inverter design tailored for PV integration to the grid which is shown in Fig. 2. Fig.1 illustrates the level-15 multilevel inverter with PV integration. Fig.2 illustrates the circuit diagram of level-15 multilevel inverter system.



**Fig. 1. Level-15 multilevel inverter with PV integration**

Pulse width modulation utilizing alternate phase opposition disposition (APOD) is a method employed in the proposed 15-level voltage to generate the required output waveform. In this technique, 14 triangular carrier signals are used in conjunction with a single sinusoidal reference signal for efficient voltage synthesis. Each of the 14 triangular carrier signals operates at different amplitudes and is out of phase with one another. These carriers are symmetrically distributed above and below the sinusoidal reference signal. When modulated using the reference sinusoidal signal, the switches in the inverter are controlled accordingly, producing

the required multilevel output voltage levels. By manipulating the widths of the pulses in the carrier signal to the sinusoidal reference signal, the MLI generates the desired stepped voltage waveform. The precise width modulation across the carriers achieves multiple voltage levels, offering a higher resolution in approximating the sinusoidal waveform. APOD PWM technique ensures balanced switching among the various voltage levels, reducing harmonic content and improving the quality of the output voltage. This method allows for smooth control over the output voltage, resulting in reduced THD and enhanced efficiency in power conversion. The combination of multiple carriers and a single sinusoidal reference facilitates the generation of a high-quality multilevel output waveform essential for applications requiring clean and efficient power, such as grid-connected renewable energy systems. Fig. 3 illustrates the PWM with alternate phase opposition disposition. Table 1 illustrates the PWM switching pattern of seven switches with 15 level output. Three asymmetrical voltages,  $V_1 = 46\text{V}$ ,  $V_2 = 92\text{V}$ , and  $V_3 = 184\text{V}$ , are applied to an inverter topology. When switches  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$ , and  $S_7$  are turned on, the cumulative voltage of 322V is calculated based on the voltage equation. Similarly, the other voltage levels are calculated accordingly.

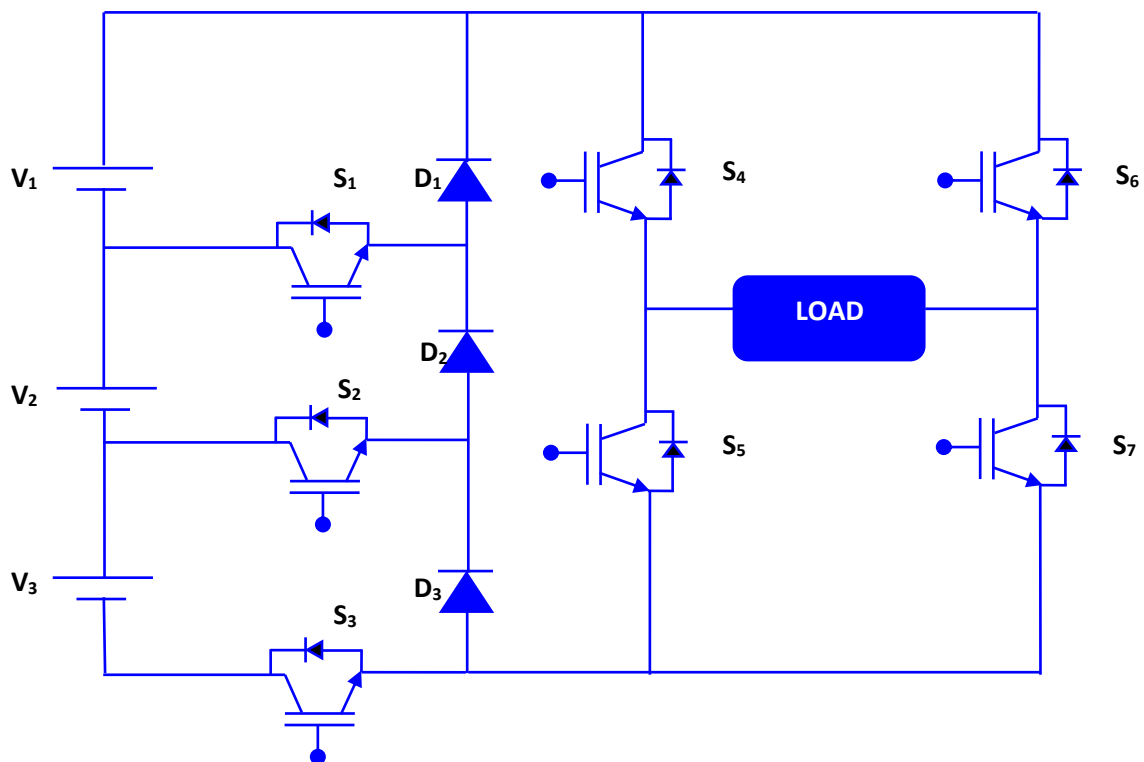
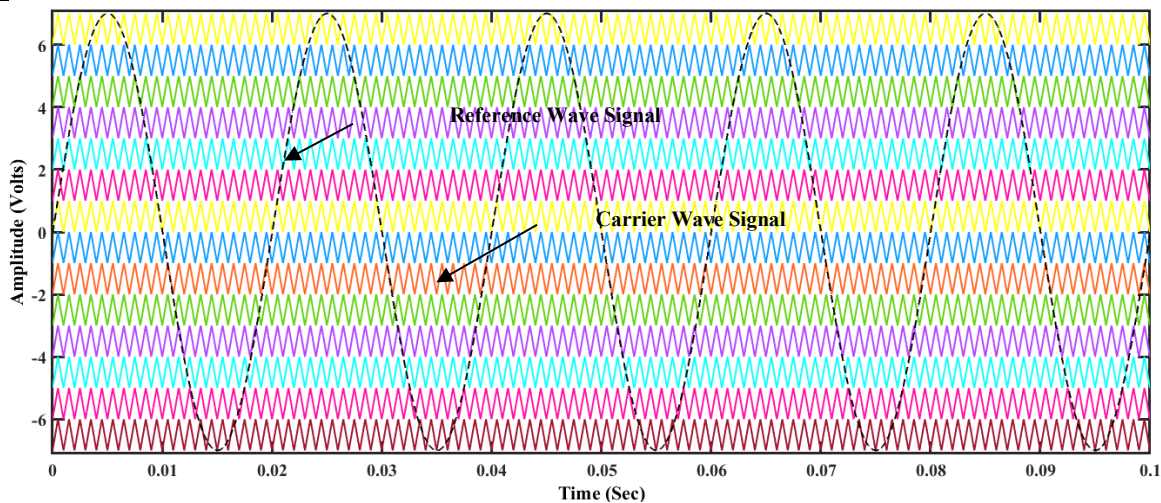


Fig. 2. Proposed level-15 inverter topology

**Table 1. Fifteen level inverter switching table**

Level	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	S <sub>5</sub>	S <sub>6</sub>	S <sub>7</sub>	Cumulative Voltage	Output Voltage in volts
1	1	1	1	1	0	0	1	$V_1+V_2+V_3$	322
2	0	1	1	1	0	0	1	$V_2+V_3$	276
3	1	0	1	1	0	0	1	$V_1+V_3$	230
4	0	1	1	1	0	0	1	$V_3$	184
5	1	1	0	1	0	0	1	$V_1+V_2$	138
6	0	1	0	1	0	0	1	$V_2$	92
7	1	0	0	1	0	0	1	$V_1$	46
8	0	0	0	0	1	1	0	0	0
9	1	0	0	0	1	1	0	$-V_1$	-46
10	0	1	0	0	1	1	0	$-V_2$	-92
11	1	1	0	0	1	1	0	$-(V_1+V_2)$	-138
12	0	0	1	0	1	1	0	$-V_3$	-184
13	1	0	1	0	1	1	0	$-(V_1+V_3)$	-230
14	0	1	1	0	1	1	0	$-(V_2+V_3)$	-276
15	1	1	1	0	1	1	0	$-(V_1+V_2+V_3)$	-322

**Fig. 3. PWM with alternate phase opposition disposition**

### 3. RESULTS AND DISCUSSION

Fig. 5 illustrates the 15-level Simulink model with 7 insulated gate bipolar transistor (IGBT) power switches with PV regulators. In this comprehensive analysis, Figs 6 and 7 illustrate the I-V (current-voltage) and P-V (power-voltage) characteristics, respectively, of the photovoltaic array, showcasing its operational range spanning from 59.16 to 11.11 volts. These graphs provide insights into the PV array's behavior under varying operating conditions. Figs. 8 and 9 exhibit the voltage and current outputs generated by the fifteen-level inverter under resistive and resistive-inductive loads, respectively. These outputs are maintained at 230 volts and 8 amperes in the case of the resistive-inductive load, indicating the inverter's performance under specific load conditions. Fig.10 illustrates the conventional converter performance parameters

which is compared to proposed converter. Fig.11 illustrates the total harmonic distortion of current harmonics produced by the fifteen-level inverter, indicating the extent of distortion at 230 volts and 7 amperes, crucial for assessing waveform quality. The voltage harmonics remain constant at 14.23% with or without filtering. However, after filtering the output current with an inductor, the THD decreases significantly from 14.23% to 3.91%. This reduction is attributed to the inductive effect occurring both before and after the filtering operation. Table 3 illustrates the performance parameters of conventional and proposed H- Bridged. Fig.12 illustrates the efficiency comparative analysis various 15 level inverter.

The I-V characteristics of the solar cell circuit are able to controlled using the subsequent Eq.1, and 2 (Sarebanzadeh, 2021). The diode's current is supplied by the following:

$$I_D = I_0 [\exp(q(V + IR_s) / KT) - 1] \tag{1}$$

$$I = I_L - I_D - I_{sh} \tag{2}$$

$$I = I_L - I_0 [\exp(q(V + IR_s) / KT) - 1] - (V + IR_s) / R_{sh} \tag{3}$$

Similar in which current harmonics are computed as equation (3), the voltage total harmonic distortion of the proposed MLI is determined using the following equation, where  $V_1$  is the fundamental root mean square (RMS) voltage and  $V_2, V_3, \dots, V_n$  are the RMS voltage of the nth harmonics. Similarly, current total harmonics are also computed,

$$THD = \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2}{V_1^2}} \tag{3}$$

In the proposed design, massive power losses were localized in three main locations and mostly happened during the conduction and switching phases. These losses (Al-Hitmi, 2023; Anssari, 2021; Suresh et al, 2023) have a major effect on overall effectiveness. Thus, the multilayer inverter's (MLI) overall power loss can be represented by the following Eq.4.

$$W_{Loss} = W_{Switching} + W_{Conduction} \tag{4}$$

The expression which follows (5) is used to determine the conduction loss of power semiconductor devices,

$$W_{Conduction} = \int_0^{T_0/2} \left\{ [V_{CEO} + r i_p \sin(\omega t)] * i_p \sin(\omega t) \left[ \frac{1}{2} (1 + A_m \sin(\omega t + \varphi)) \right] dt \right\}$$

Following the simplification of the above expression,

$$W_{Conduction} = \frac{1}{2} \left\{ \left( V_{CEO} * \frac{i_p}{\pi} + r * \frac{i_p^2}{4} \right) + \left( A_m * \cos\varphi * V_{CEO} * \frac{i_p}{8} \right) + \left( \frac{1}{3\pi} * r i_p^2 \right) \right\} \tag{5}$$

where  $i_p$  is the IGBT device's peak current,  $r$  is the collector to emitter on-state resistance,  $A_m$  is the modulation index, and  $V_{CEO}$  is the zero-current collector (Khoun-Jahan, 2021; Liu et al, 2022) to emitter voltage. Switching loss refers to the total energy dissipated during the transition

periods when a power device turns on and off. Variable switching time is taken into account and included into Eq.6.

$$W_{Switching} = f_{sw} \frac{1}{T_0} \int_0^{T_0/2} (E_{on} + E_{off})(t, i_p) dt \quad (6)$$

Where  $E_{on}$  is the on-state voltage drop,  $E_{off}$  is the off-state voltage drop,  $T_0$  is the switching time period, and  $f_{sw}$  is the switching frequency. The following formula is used to determine MLI's efficiency in Eq.7.

$$Efficiency = \frac{P_{Output}}{P_{Output} + W_{Loss}} * 100 \quad (7)$$

The output voltage rises as the converter's duty cycle increases and decreases as its duty cycle decreases.

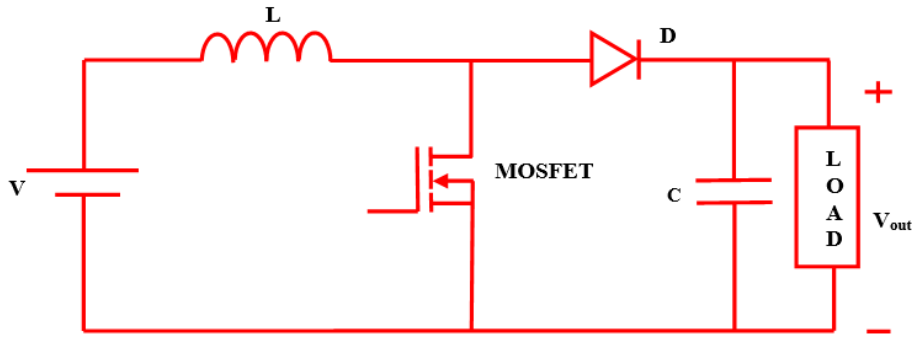


Fig.4. DC - DC Boost converter circuit

Table 2. Parameters of boost converter

Parameters	Values
Duty cycle	90%
Switching Frequency	5kHz
Output voltage	230 Volts
Input voltage	24 Volts
Inductor	3.34 mH
Capacitor	7.48 $\mu$ F
Capacitor voltage (Ripple)	29.98%
Inductor current (Ripple)	4.95%

The following expressions (8) and (9) are used for designing the boost converter inductor (L) and capacitor (C) values,

$$L = \frac{V_{min} * D}{f_s * I_L} \quad (8)$$

$$C = \frac{I_{max} * D}{f_s * \Delta V_c} \quad (9)$$

The design values of the boost converter that connects the PV panel and inverter system are shown in Table 2. The boost converter circuit shown in Fig.4 is widely used in a variety of

applications, including electronic power supply, battery-operated devices, renewable energy systems, and DC-to-DC voltage conversion. They are particularly useful in applications where the input voltage is lower than the required output voltage since they can step up the voltage to the necessary level.

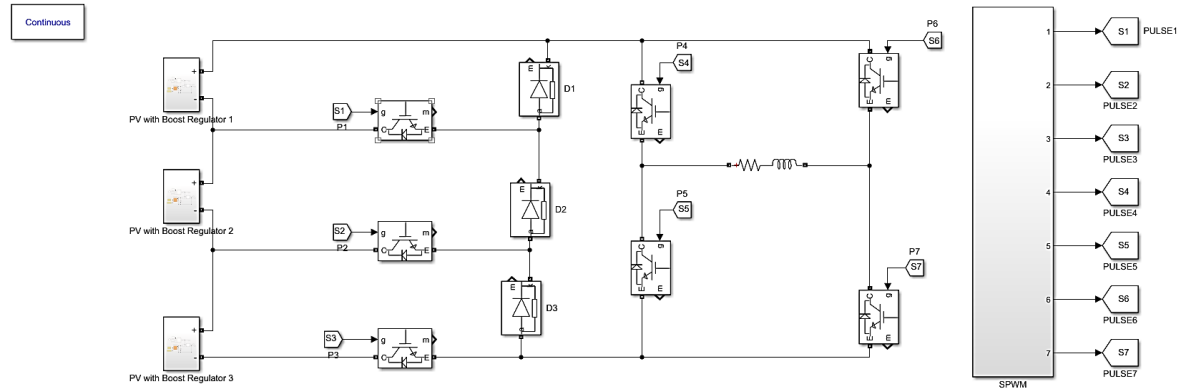


Fig. 5. Simulink model of level-15 inverter

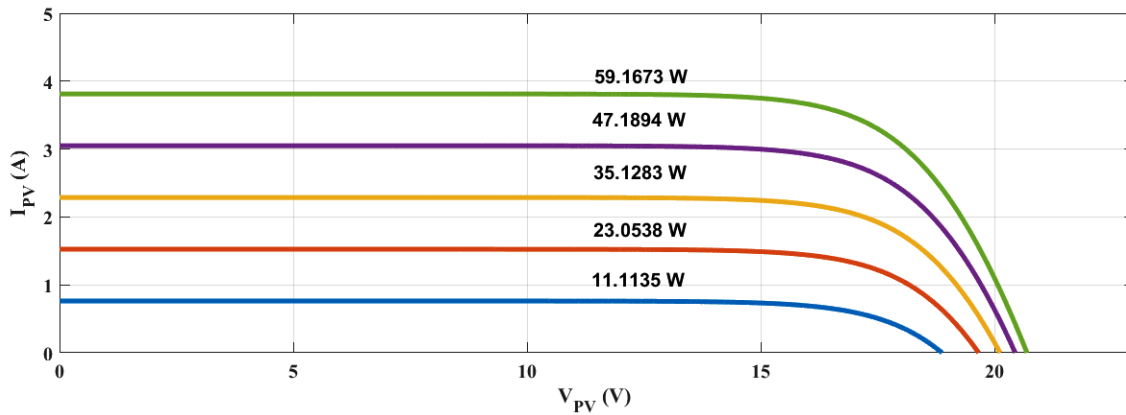


Fig. 6. PV array I-V characteristics

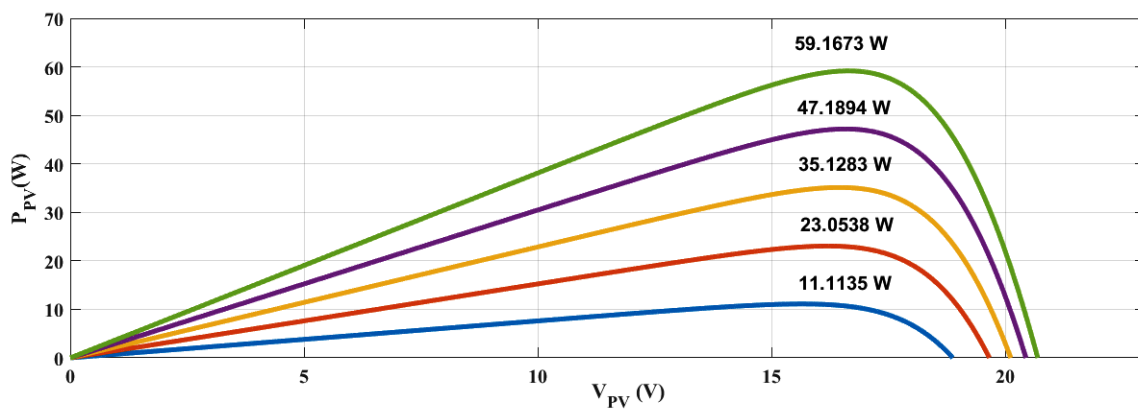
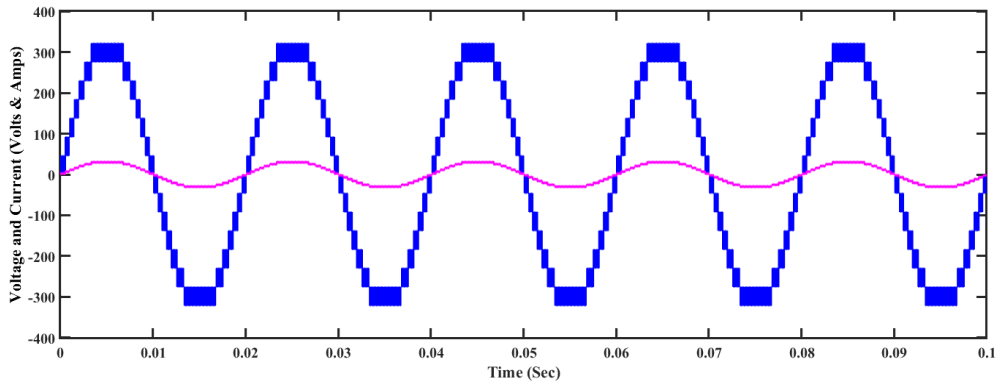
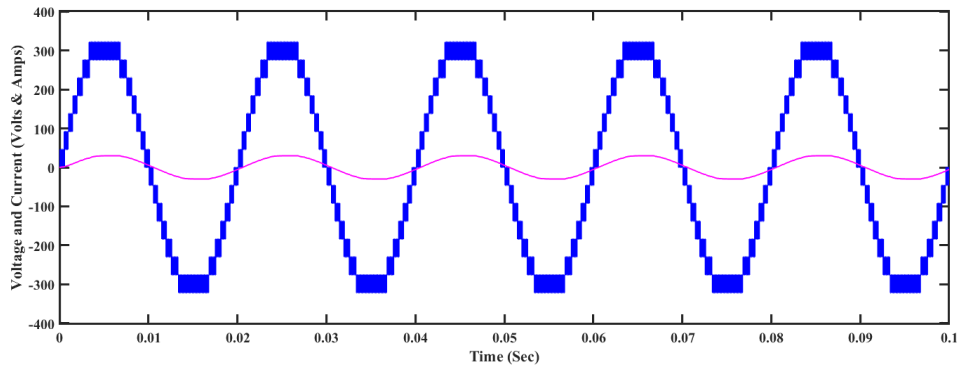


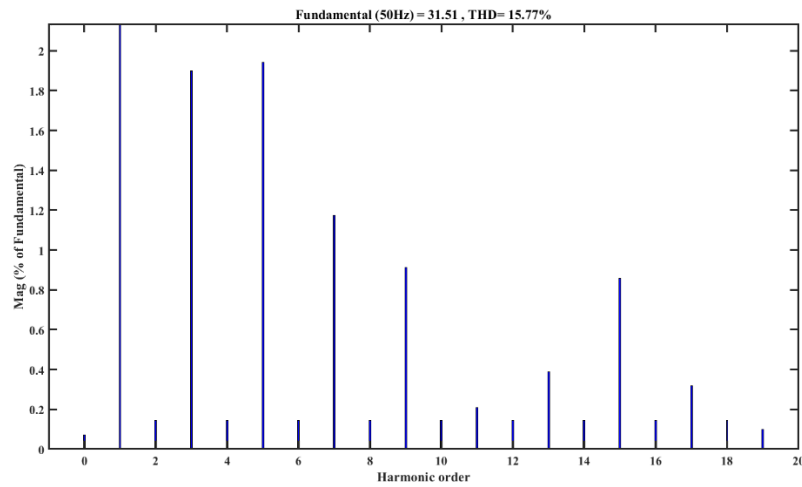
Fig. 7. PV array P-V characteristics



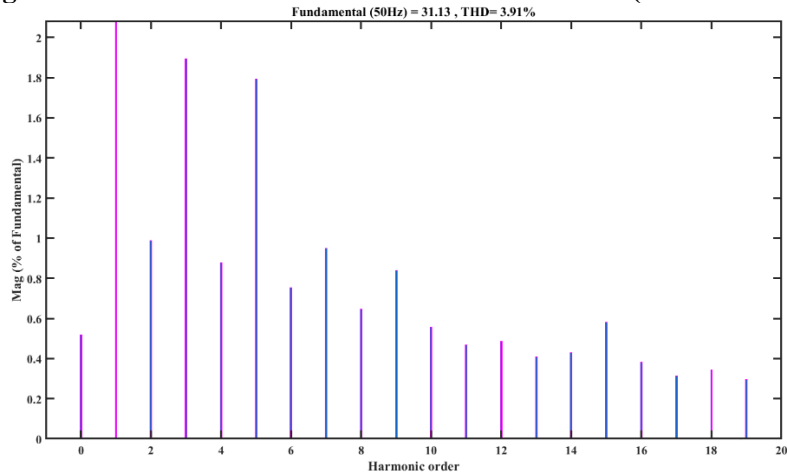
**Fig. 8. Voltage and current output of level-15 inverter with resistive load**



**Fig. 9. Voltage and current output of level-15 inverter with resistive inductive load**



**Fig. 10. THD current harmonics of level-15 inverter (Conventional)**



**Fig. 11. THD current harmonics of level-15 inverter (Proposed)**

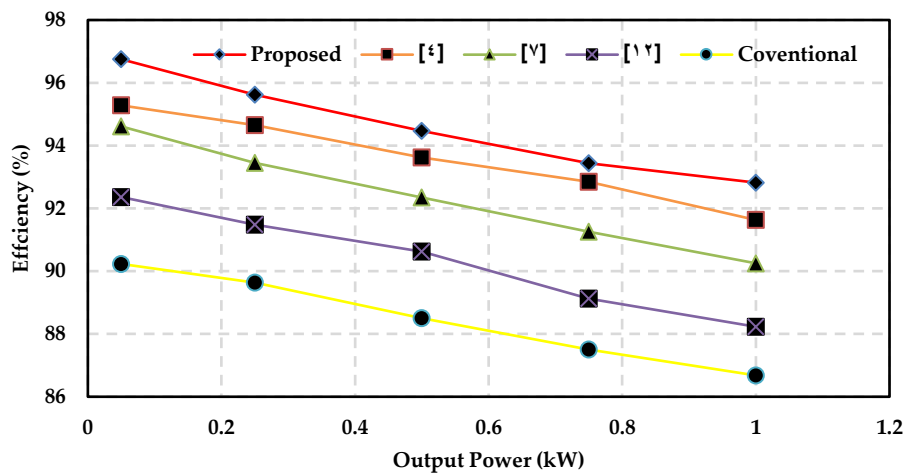


Fig. 12. Efficiency comparisons of various level-15 inverter

Table 3. Performance parameters of Conventional and proposed H- Bridged

Parameters	Conventional H - Bridged	Proposed H - Bridged
DC Sources (Nos)	7	3
Supply	32 V	32 V
AC output voltage	230 V	230 V
No. of IGBTs	20	7
Driver Circuits	20	7
Carrier frequency	2400Hz	2400Hz
%THD (Current)	15.77 (RL load)	3.91 (RL load)
Efficiency	90.23 %	96.75

#### 4. CONCLUSIONS

This advanced 15-level inverter design showcases a remarkable improvement in integrating solar PV systems into the grid. The achieved THD values of 3.91% for current and 15.77% for voltage signify substantial enhancements in waveform quality, underscoring the inverter's capacity to produce cleaner and more efficient power. Accomplishing an impressive efficiency rating of 96.75% signifies a notable advancement in power conversion efficacy compared to traditional systems. The reduction in the switch count to seven emphasizes cost-effectiveness and operational simplicity, essential for practical deployment in real-world applications. Through extensive MATLAB/Simulink simulations, diverse operational scenarios were rigorously assessed, emphasizing seamless PV integration with the grid. The results demonstrated favorable outcomes in terms of stability, reliability, and grid interaction, solidifying the proposed inverter system's practical viability. Furthermore, in future work, enhanced grid integration and reliability will be emphasized through rigorous simulation studies, ensuring practical deployment feasibility in diverse operational environments.

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