Kufa Journal of Engineering
Vol. 9, No. 4, October 2018, P.P. 210-219
Received 8 October 2017, accepted 17 January 2018

A NEW STRUCTURE OF FIVE-LEVEL DIODE CLAMPED INVERTER WITH REDUCING ITS ELEMENTS

Othman M. Anssari[1]

[1]Assistant lecture, University of Kufa, Information Technology Research and Development Center, othman.alansari@uokufa.edu.iq

http://dx.doi.org/10.30572/2018/kje/090414

ABSTRACT

At the high power switching circuit's applications, when the harmonic distortion is harmful, a multi-level diode clamped inverter is useful, especially when reduced total harmonic distortion and high power are desired. But when the levels get a rise, number of semiconductors are also rising, which leads to many problems such as increasing cost, losses, installation area, and total harmonic distortion. Many researchers have tried to find solutions to these problems. In this sense, this paper focuses on: a) build a new structure of five level diode clamped inverter. b) Increase the efficiency of the inverter by reducing the number of switches. c) Reduce the total harmonic distortion.

The theoretical calculation and simulation results are performed for five level diode clamped inverter by MATLAB/ SIMULINK.

KEYWORDS: Five level diode clamped inverter, Direct pulse generator, THD.

1. INTRODUCTION

A multi-level invertor was lunched in the seventies of the previous century. Using of multi-level invertor was limited to simple levels. With the developing of time and the increasing applications, the multi-level inverter evolved and the electronic circuits developed to have complex forms and higher levels.

The power electronics have pushed major awareness to multi-level inverters as a novel kind of power converters. Multi-level inverters divided into three topologies, flying capacitors inverter (Kou, 2003), diode clamped inverter (Chen, 2006, Bender, 2006 and Cheng 2006), and cascade H bridge inverter (Zhang, 2001, Watson, 2007, Malinowski, 2009). These three types commonly depend on the source of the voltages. There are other types which rely on the adopted source as the source of current (Shen, 2002).

Many research articles have found in the literature about the multi-level diode clamped inverter. For examples, these research papers published by (Rodriguez et al. 2010, Jayasinghe et al. 2011, Chaturvedi et al. 2011). Fig. 1 shows the three level diode clamped inverter as an example.

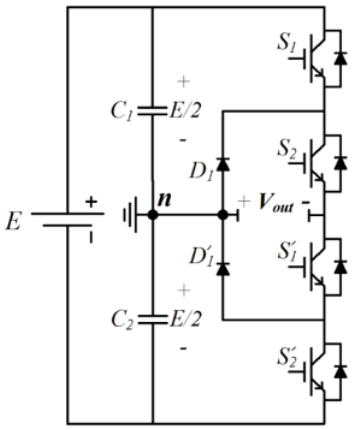

Fig. 1. Three Level Diode Clamped Inverter.

The main reason for using multi-level inverters is to lower voltage compression on the switches, relegate of electromagnetic interference trouble, and reduce harmonics, and reduce losses (Rodriguez, 2002). The multi-level diode clamped inverter is frequently used in many applications because it provides a high efficiency for switching at the fundamental frequency. The benefit of using diode because it gives a finite value of voltage leading to reduce compression on the devices. However, there are few disadvantages of using diode clamped inverter. For example, when the levels get rise more than three levels or five levels, it will be

difficult due to that it needs more and more elements (diodes, capacitors, and switches), which leads to increase in switching losses and cost. In addition to complexity in switching control and structure (Newton, 1998; Yuan, 1998). Many research have been done to overcome these drawbacks.

2. MULTI-LEVEL DIODE CLAMPED INVERTER (BACKGROUND)

Normally the main circuit of the n- level diode clamped inverter has [2(n-1)] switches, [(n-1)] capacitor, and [(n-1) (n-2)] diodes (Yuan, 2000). So, the five-level diode clamped inverter can be configured as shown in the Fig. 2. By using eight switches, four capacitors, and twelve diodes, capacitor voltage balancing, and regulation are investigated (Ishida, 2002; Pan, 2005).

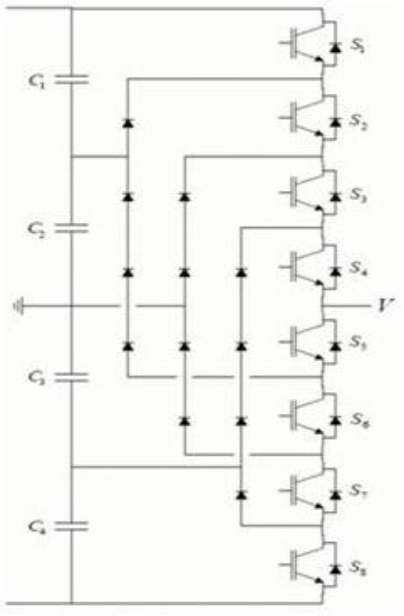

Fig. 2. Five Level Clamped Inverter.

Here, the dc voltage source considered as a constant. The voltage in every capacitor is considered the same. Thus, voltage compression on every switch is ($V_{dc/4}$). Table 1 lists the modes of switches to the five-level diode clamped inverter with the magnitude of the output voltage. Each mode has four switches (ON) and four switches (OFF). Number one indicates that the switch is ON and zero indicates that switch is OFF. By changing these modes, different output can be achieved.

3. PROPOSED FIVE LEVEL DIODE CLAMPED INVERTER

A proposed five level diode clamped inverter has six switches, four capacitors, and six diodes as shown in Fig. 3. The proposed inverter gives same levels with less elements. Here, the dc

bus voltage divided into five levels by four capacitors connected in series C1 to C4. Center point n can be defined as a neutral point.

Table 1. Switching Sequence for Five Level Inverter and the magnitude of The Output Voltage.

Switch no.	Output voltage				
	$V_{dc/2}$	$V_{dc/4}$	Zero	$-V_{dc/2}$	$-V_{dc/4}$
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	0	1	1	1	1
6	0	0	1	1	1
7	0	0	0	1	1
8	0	0	0	0	1

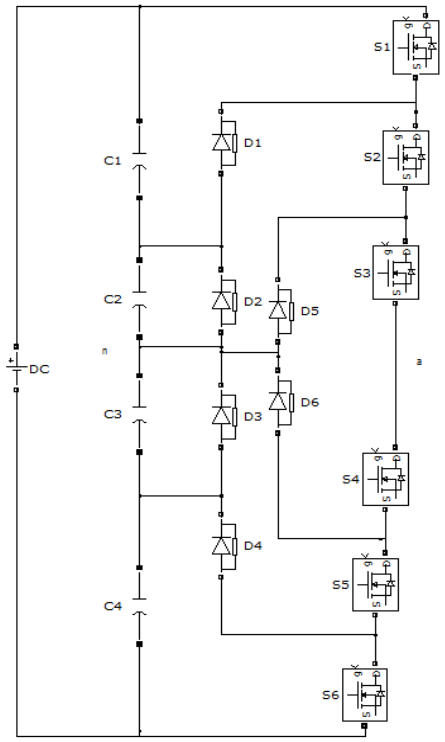

Fig. 3. Proposed Five Level Diode Clamped Inverter

Switching planner is used to guarantee that switches work in tangent modes. (Van) is the output voltage has five cases ($V_{dc/2}$), ($V_{dc/4}$), (0), ($-V_{dc/4}$), ($-V_{dc/2}$) as shown in Fig. 4.

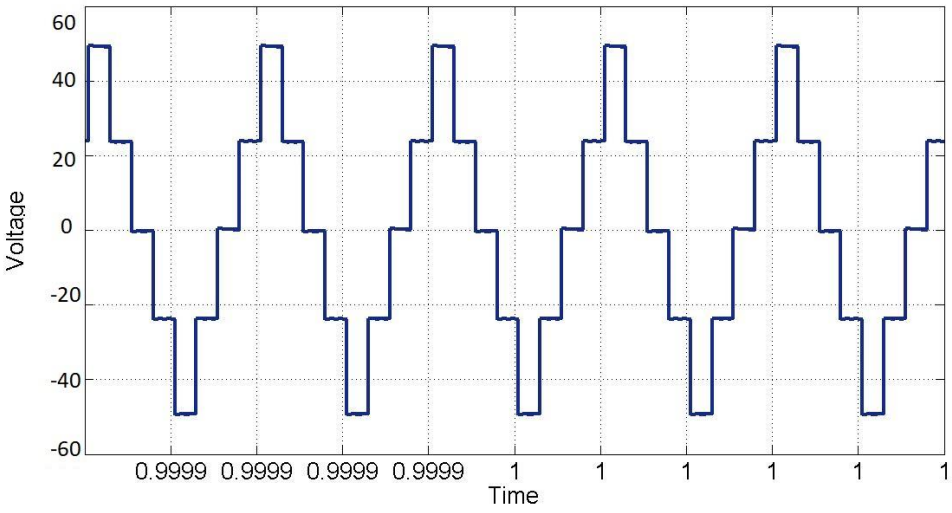

Fig. 4. Output Voltage Proposed Five Level Diode Clamped Inverter.

Output voltage $V_{dc/2}$ generated when switches 1,2 and 3 are ON, switches 4,5 and 6 are OFF. $V_{dc/4}$ generated when switches 2 and 3 are ON, switches 1,4,5 and 6 are OFF. Zero voltage generated when switches 3 and 4 are ON, switches 1,2,5 and 6 are OFF. $-V_{dc/2}$ generated when switches 4 and 5 are ON, switches 1,2,3 and 6 are OFF. $-V_{dc/4}$ generated when switches 4,5 and 6 are ON, switches 1,2 and 3 are OFF, as listed in Table 2. The most popular way is pulse width modulation (Yuan, 2000; Chaturvedi et al., 2011; Jayasinghe et al., 2011). Using direct pulse generator in proposed inverter by depending on the next table.

Table 2. Switching Sequence Proposed Five Level Diode Clamped Inverter and the magnitude of The Output Voltage.

Switch no.	Output voltage				
	$V_{dc/2}$	**$V_{dc/4}$**	**zero**	**$-V_{dc/2}$**	$-V_{dc/4}$
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	0	0	1	1	1
5	0	0	0	1	1
6	0	0	0	0	1

Providing a square wave at constant intervals in MATLAB program called pulse generator, by using source block parameters for each switch, depending on Table 2, choosing the phase

delay, period and pulse width for switch 1, then switch 1 has one time ON at $V_{dc/2}$ and OFF for all other times in period, thus it works for 20% (periodicity for each cycle).

Switch 1 works at first column without any delay, therefor phase delay is zero (work directly with first pulse) and so on for all switches as shown in Fig. 5. Putting these parameters for all switches depending on table 2 to get the desirable output voltage.

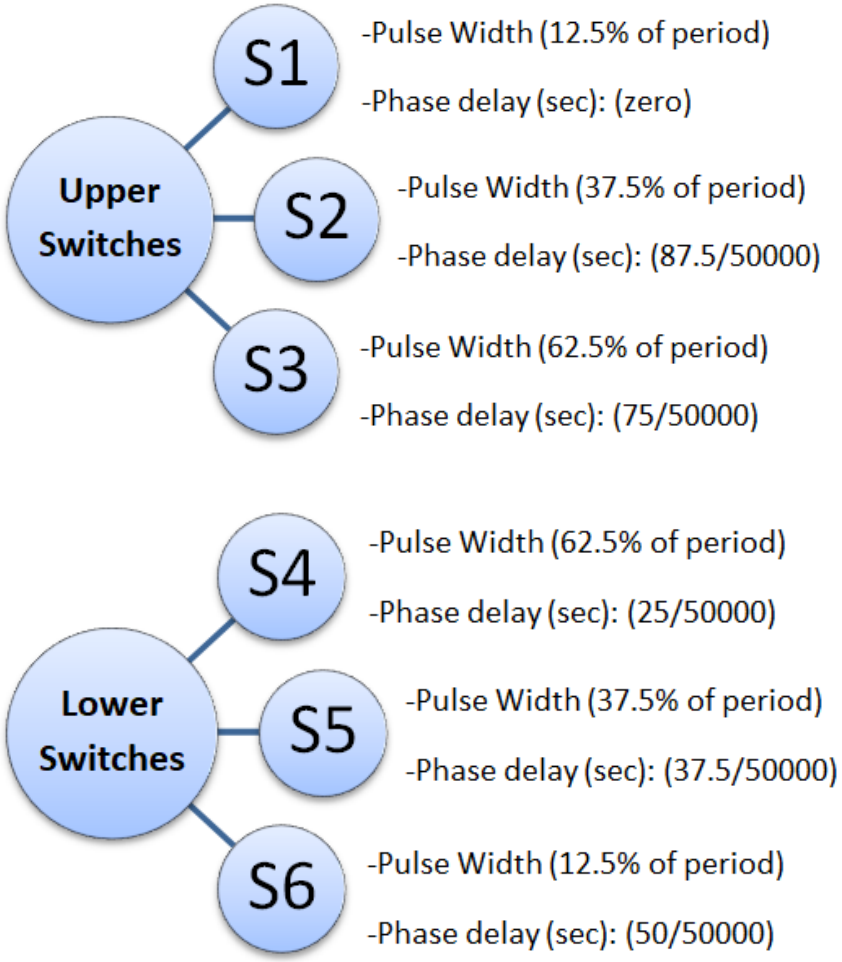

Fig. 5. Pulse width and Phase delay for Upper and Lower Switches.

This inverter prepared according to the next specifications:-

Input voltage V_{dc}= 100 volt

Capacitors 100 µ Farad

Switching frequency f_{sw}= 50 KHZ

Output voltage 100 volt pk-pk

$V_{dc}= V_{c1}+V_{c2}+V_{c3}+V_{c4}$ 1

$$V_{c1}= V_{c2}= V_{c3}= V_{c4=} V_{dc}/4 \quad (2)$$

Period time (sec) for switching On= $1/f_{sw.}$

The new structure of five-level diode clamped inverter lowering Total Harmonic Distortion (THD) from output voltage waveforms, THD for the classical five-level diode clamped inverter is about 29.60 % and the proposed diode clamped inverter can generate five level at the output with total harmonic distortion (THD) of only 25.31% as shown in Fig. 6 and 7.

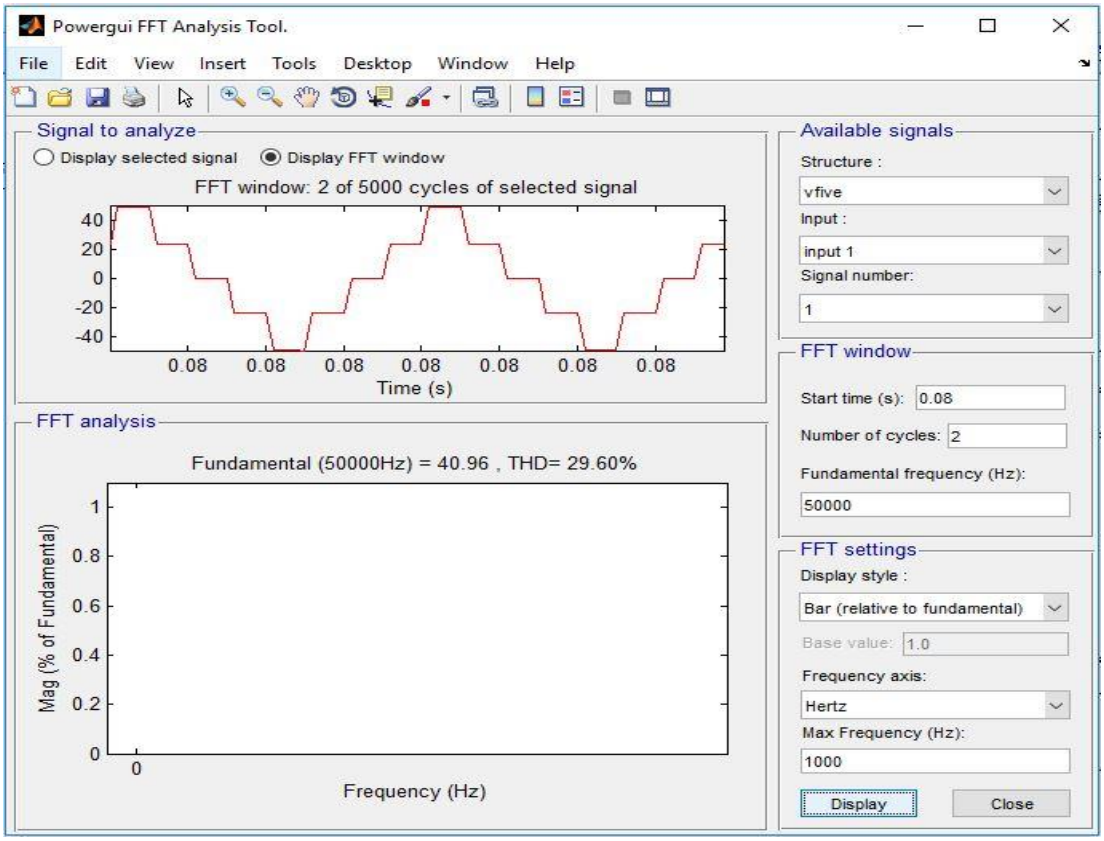

Fig. 6. THD for the Classical Five Level Diode clamped Inverter.

Table 3 shows the comparison between the classical and the proposed topology of five level diode clamped inverter. The proposed inverter gives same levels with less elements and lower THD.

Table 3. Comparison between Classical and Proposed Topology Five Level Diode Clamped Inverter

Topology	No. of Switches	No. of Diodes	THD %
Classic topology	8	12	29.60
Proposed topology	6	6	25.31

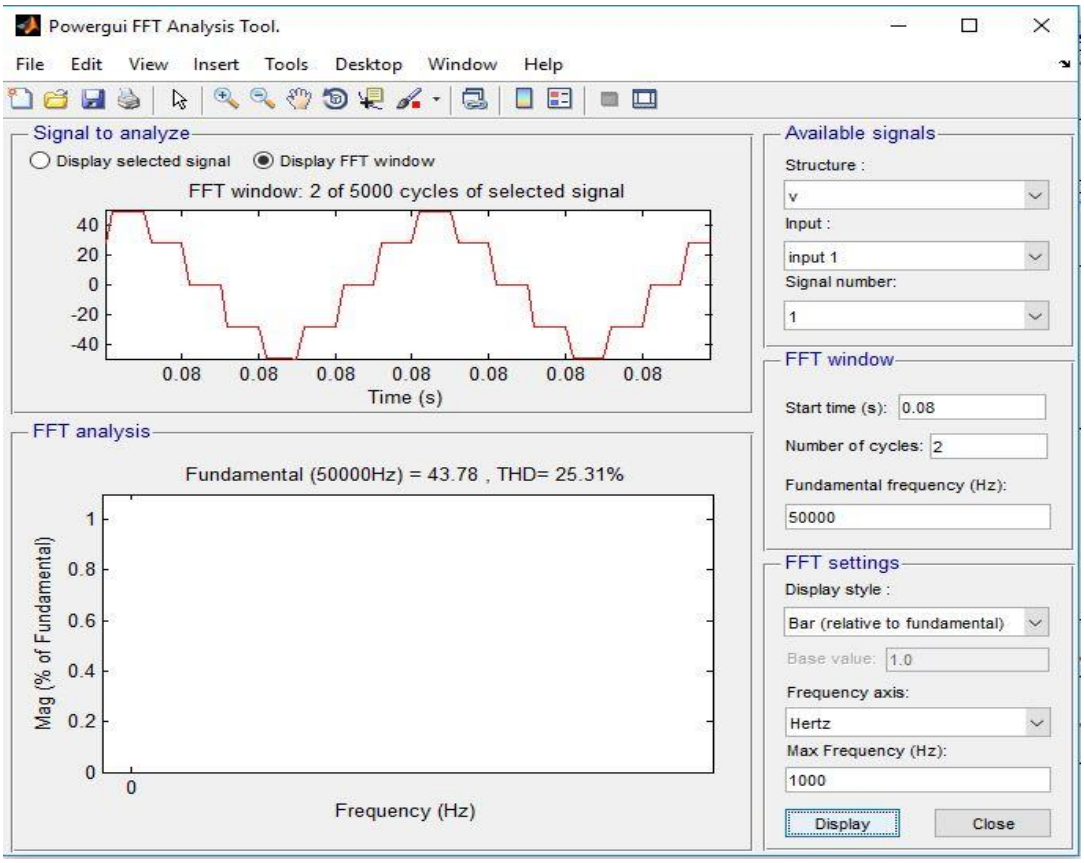

Fig. 7. THD for the Proposed Five Level Diode clamped Inverter.

4. CONCLUSION

A multi-level diode clamped inverter is useful to be used in the high power applications, especially when reducing total harmonic distortion and high power are desired**.**

When the levels get rise, number of semiconductors are rise also. This drives to many problems such as increasing cost, losses, installation area and total harmonic distortion**.**

The proposed five-level diode clamped inverter solve all the previous problems. It can produce same number of voltage levels with lower number of elements (switches and diodes) and lower total harmonic distortions compared to the classical inverters.

By using least number of switches and gate trigger circuits, there by guarantee the minimum switching losses, reducing size, installation cost, and maximum efficiency.

5. REFERENCES

Bendre, G., Venkataramanan, D., Rosene, V., and Srini-Vasan, Modeling and Design of a Neutral-Point Voltage Regulator for a Three-Level Diode-Clamp Inverter Using Multiple-Carrier Modulation, IEEE Transaction on Industrial Electronics, Vol. 53, No. 3, 2006, pp. 718- 726.

Chen, A. and He, X., 2006 “Research on Hybrid-Clamp Multi-Level Inverter Topologies”, IEEE Transaction on Industrial Electronics, Vol. 53, No. 6, pp. 1898-1907.

Watson, A. J., Wheeler, P. W. and Clare, J. C., 2007 “A Complete Harmonic Elimination Approach to DC Link Voltage Balancing for a Cascade Multi-level Rectifier”, IEEE Transactions on Industrial Electronics, Vol. 54, No. 6, pp. 2946-2953.

Newton, C. and Sumner, M., 1998 “Multi-level Converters: A Real Solution to Medium High Voltage Drives”, Inst. Electron. Eng.—Power Eng. J., pp. 21–26, Feb.

Chaturvedi, P. K., S. Jain, and P. Agarwal. Reduced Switching Loss Pulse Width Modulation Technique for Three-Level Diode Clamped Inverter. IET Power Electronics 4.4 (2011): 393-399.

Zhang, J., Zou, Y., Zhang, X. and Ding, K., Study on a Modified Multi-level Cascade Inverter with Hybrid Modulation, 4th International Conference on Power Electronics and Drive System, Bali, 22-25 October 2001, pp. 379-383.

Jayasinghe, S. D., Gamini, D. Mahinda, Vilathgamuwa, and Udaya, K. Madawala. “Diode-Clamped Three-Level Inverter-Based Battery/ Super Capacitor Direct Integration Scheme for Renewable Energy Systems”. IEEE Transactions on Power Electronics 26.12 (2011): 3720-3729.

Kou, Xiaomin, Keith A. Corzine, and Familiant, Y. “A Unique Fault-Tolerant Design for Flying Capacitor Multi-Level Inverters”. IEEE International Conference in Electric Machines and Drives, IEMDC'03.. Vol. 1. 2003.

M. Malinowski, K. Gopakumar, J. Rodriguez and M. Perez, A Survey on Cascade Multi-level Inverters, IEEE Transactions on Industrial Electronics, Vol. 57, No. 7, 2009, pp. 2197-2206.

Rodriguez, Jose, 2010, “A Survey on Neutral-Point-Clamped Inverters”. IEEE transactions on Industrial Electronics 57.7, 2219-2230.

Rodriguez, Jose, Jih-Sheng Lai, and Fang Zheng Peng, 2002, “Multi-level Inverters: A Survey of Topologies, Controls and Applications”. IEEE Transactions on industrial electronics 49.4: 724-738.

Shen, Dong, and Lehn P. W., 2002, “Modeling, Analysis and Control of a Current Source Inverter-based STATCOM”. IEEE Transactions on power delivery 17.1, 248-253.

Ishida, T., Matsuse, K., Sasagawa, T. M. K., and Huang, L., 2002, "Fundamental Characteristics of Five-level Double Converter with Adjustable dc Voltage for Induction Motor Drive", IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 775–782.

Yuan, X., "Soft Switching Techniques for Multi-level Invreters", Ph.D. thesis, INEP-UFSC, Brazil, May 1998.

Cheng, Y., Qian, C., Crow, M. L., Pekarek, S., and Atcitty, S., 2006, "A Comparison of Diode-Clamp and Cascade Multi-level Converters for a STATCOM with Energy Storage", IEEE Transactions on Industrial Electronics, Vol. 53, No. 5, pp. 1512-1521.

Yuan, Xiaoming, and Ivo Barbi. 2000, "Fundamentals of a New Diode Clamping Multi-level Inverter". IEEE Transactions on power electronics 15.4 (): 711-718.

Pan, Z., Peng, F. Z., Corzine, K. A., Stefanovic, V. R., Leuthen, J. M., and Gataric, S., 2005, "Voltage Balancing Control of Diode Clamp Multi-level Rectifier/ Inverter Systems", IEEE Trans. Ind. Appl., vol. 41, no. 6, pp. 1698–1706.